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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Low Profile Chip Scale Stacking System and Method

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Examiner: To be assigned

Group: To be assigned

Related Applications:

[001] This application is a continuation-in-part of U.S. Pat. App. No. 10/453,398, filed June 3, 2003, pending, which is a continuation-in-part of U.S. Pat. App. No. 10/005,581, filed October 26, 2001, now U.S. Pat. No. 6,576,992 B2, issued June 10, 2003, both of which applications are hereby incorporated by reference in their entirety, and this application is a continuation-in-part of U.S. Pat. App. No. 10/457,608 filed June 9, 2003, pending, which is incorporated by reference in its entirety and which application is a continuation-in-part of U.S. Pat. App. No. 10/005,581, filed October 26, 2001, now U.S. Pat. App No 6,576,992 B2.

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Angelia Dedek

Technical Field:

[002] The present invention relates to aggregating integrated circuits and, in particular, to stacking integrated circuits in chip-scale packages.

Background of the Invention:

[003] A variety of techniques are used to stack packaged integrated circuits. Some methods require special packages, while other techniques stack conventional packages. In some stacks, the leads of the packaged integrated circuits are used to create a stack, while in other systems, added structures such as rails provide all or part of the interconnection between packages. In still other techniques, flexible conductors with certain characteristics are used to selectively interconnect packaged integrated circuits.

[004] The predominant package configuration employed during the past decade has encapsulated an integrated circuit (IC) in a plastic surround typically having a rectangular configuration. The enveloped integrated circuit is connected to the application environment through leads emergent from the edge periphery of the plastic encapsulation. Such "leaded packages" have been the constituent elements most commonly employed by techniques for stacking packaged integrated circuits.

[005] Leaded packages play an important role in electronics, but efforts to miniaturize electronic components and assemblies have driven development of technologies that preserve circuit board surface area. Because leaded packages have leads emergent from peripheral sides of the package, leaded packages occupy more than a minimal amount of circuit board surface area. Consequently, alternatives to leaded packages known as chip scale packaging or "CSP" have recently gained market share.

[006] CSP refers generally to packages that provide connection to an integrated circuit through a set of contacts arrayed across a major surface of the package. Instead of leads emergent from a peripheral side of the package, contacts are placed on a major surface and typically are located along the planar bottom surface of the package. The absence of "leads" on package sides renders most stacking techniques devised for leaded packages inapplicable for CSP stacking.

[007] What is needed, therefore, is a technique and system for stacking CSPs that provides a thermally efficient, reliable structure that performs well at higher frequencies but does not add excessive height to the stack yet allows production at reasonable cost with readily understood and managed materials and methods.

Summary of the Invention:

[008] The present invention stacks chip scale-packaged integrated circuits (CSPs) into low profile modules that conserve PWB or other board surface area. Although the present invention is applied most frequently to CSPs that contain one die, it may be employed with CSPs that include more than one integrated circuit die.

[009] Preferred embodiments employ low profile contact structures to provide connection between CSPs of the stacked module and between and to the flex circuitry. Low profile contacts are created by any of a variety of methods and materials including, for example, screen paste techniques and use of high temperature solders, although other application techniques and traditional solders may be employed for creating low profile contacts that may be employed in the present invention. A consolidated low profile contact structure and technique is provided for use in alternative embodiments of the present invention.

[0010] Multiple numbers of CSPs may be stacked in accordance with the present invention. The CSPs employed in stacked modules devised in accordance with the present invention are connected with flex circuitry. That flex circuitry may exhibit one or two or more conductive layers with preferred embodiments having two conductive layers.

[0011] In some preferred embodiments, a form standard provides a physical form that allows many of the varying package sizes found in the broad family of CSP packages to be used to advantage while employing a standard connective flex circuitry design. In other embodiments, a heat spreader is disposed between the CSP and the flex circuitry thus providing an improved heat transference function without the standardization of the form standard, while still other embodiments lack either a form standard or a heat spreader and may employ, for example, the flex circuitry as a heat transference material.

Summary of the Drawings:

[0012] Fig. 1 is an elevation view of a high-density circuit module devised in accordance with a preferred four-high embodiment of the present invention.

[0013] Fig. 2 is an elevation view of a stacked high-density circuit module devised in accordance with a preferred two-high embodiment of the present invention.

[0014] Fig. 3 depicts, in enlarged view, the area marked "A" in Fig. 2 in a preferred embodiment of the present invention.

[0015] Fig. 4 depicts, in enlarged view, one alternative construction for of the area marked "A" in Fig. 2.

[0016] Fig. 5 depicts in enlarged view, the area marked "B" in Fig. 2 in a preferred embodiment of the present invention.

[0017] Fig. 6 depicts, in enlarged view, a portion of a flex circuitry employed with the structure of Fig. 4 in an alternative preferred embodiment of the present invention.

[0018] Fig. 7 is an elevation view of a portion of an alternative construction step in an alternative embodiment of the present invention.

Description of Preferred Embodiments:

[0019] Fig. 1 is an elevation view of module 10 devised in accordance with a preferred embodiment of the present invention. Exemplar module 10 is comprised of four CSPs: level four CSP 12, level three CSP 14, level two CSP 16, and level one CSP 18. Each of the depicted CSPs has an upper surface 20 and a lower surface 22 and opposite lateral sides or edges 24 and 26 and include at least one integrated circuit surrounded by a body 27.

[0020] The invention is used with CSP packages of a variety of types and configurations such as, for example, those that are die-sized, as well those that are near chip-scale as well as the variety of ball grid array packages known in the art. It may also be used with those CSP-like packages that exhibit bare die connectives on one major surface. Thus, the term CSP should be broadly considered in the context of this application. The invention may be employed to advantage in the wide range of CSP configurations available in the art where an array of connective elements is available from at least one major surface. Collectively, these will be known herein as chip scale packaged integrated circuits (CSPs) and preferred embodiments will be described in terms of CSPs, but the particular configurations used in the explanatory figures are not, however, to be construed as limiting. For example, the elevation views of Figs. 1 and 2 are depicted with CSPs of a particular profile known to those in the art, but it should be understood that the figures are exemplary only. For example, in Fig. 7, a CSP is shown that has a

profile different than the profile of the CSPs shown in Figs 1 and 2. The invention is advantageously employed with CSPs that contain memory circuits, but may be employed to advantage with logic and computing circuits where added capacity without commensurate PWB or other board surface area consumption is desired.

[0021] Shown in Fig. 1 are low profile contacts 28 along lower surfaces 22 of the illustrated constituent CSPs 12, 14, 16, and 18. Low profile contacts 28 provide connection to the integrated circuit or circuits within the respective packages.

[0022] CSPs often exhibit an array of balls along lower surface 22. Such ball contacts are typically solder ball-like structures appended to contact pads arrayed along lower surface 22. In many preferred embodiments of the present invention, CSPs that exhibit balls along lower surface 22 are processed to strip the balls from lower surface 22 or, alternatively, CSPs that do not have ball contacts or other contacts of appreciable height are employed. Only as a further example of the variety of contacts that may be employed in alternative preferred embodiments of the present invention, an embodiment is later disclosed in Fig. 4 and the accompanying text that is constructed using a CSP that exhibits ball contacts along lower surface 22. The ball contacts are then reflowed to create what will be called a consolidated contact.

[0023] Embodiments of the invention may also be devised that employ both standard ball contacts and low profile contacts or consolidated contacts. For example, in the place of low profile inter-flex contacts 42 or, in the place of low profile contacts 28, or in various combinations of those structures, standard ball contacts may be employed at some levels of module 10, while low profile contacts and/or low profile inter-flex contacts or consolidated contacts are used at other levels.

[0024] A typical eutectic ball found on a typical CSP memory device is approximately 15 mils in height. After solder reflow, such a ball contact will typically have a height of about 10 mils. In preferred modes of the present invention, low profile contacts 28 and/or low profile inter-flex contacts 42 have a height of approximately 7 mils or less and, more preferably, less than 5 mils.

[0025] Where present, the contact sites of a CSP that are typically found under or within the ball contacts typically provided on a CSP, participate in the creation of low profile contacts 28. One set of methods by which high-temperature types of low profile contacts 28 suitable for use in embodiments of the present invention are created is disclosed in co-pending and incorporated U.S. Pat. App. No. 10/457,608 filed June 9, 2003. In other embodiments, more typical solders, in paste form for example, may be applied either to the exposed contact sites or pads along lower surface 22 of a CSP and/or to the appropriate flex contact sites of the designated flex circuit to be employed with that CSP.

[0026] In Fig. 1, iterations of flex circuits ("flex", "flex circuits," "flexible circuit structures," "flexible circuitry") 30 and 32 are shown connecting various constituent CSPs. Any flexible or conformable substrate with an internal layer connectivity capability may be used as a preferable flex circuit in the invention. The entire flex circuit may be flexible or, as those of skill in the art will recognize, a PCB structure made flexible in certain areas to allow conformability around CSPs and rigid in other areas for planarity along CSP surfaces may be employed as an alternative flex circuit in the present invention. For example, structures known as rigid-flex may be employed.

[0027] Form standard 34 is shown disposed adjacent to upper surface 20 of each of the CSPs below level four CSP 12. Form standard 34 may be fixed to upper surface 20 of the respective CSP with an adhesive 36 which preferably is thermally conductive. Form standard 34 may also, in alternative embodiments, merely lay on

upper surface 20 or be separated from upper surface 20 by an air gap or medium such as a thermal slug or non-thermal layer.

[0028] In other embodiments, a heat spreader may act as a heat transference media and reside between the flex circuitry and the package body 27 or may be used in place of form standard 34. Such a heat spreader is shown in Fig. 7 as an example and is identified by reference numeral 37. In still other embodiments, there will be no heat spreader 37 or form standard 34 and the embodiment may use the flex circuitry as a heat transference material.

[0029] With continuing reference to Fig. 1, form standard 34 is, in a preferred embodiment, devised from copper to create, as shown in the depicted preferred embodiment of Fig. 1, a mandrel that mitigates thermal accumulation while providing a standard-sized form about which flex circuitry is disposed. Form standard 34 may take other shapes and forms such as, for example, an angular "cap" that rests upon the respective CSP body. Form standard 34 also need not be thermally enhancing although such attributes are preferable. The form standard 34 allows modules 10 to be devised with CSPs of varying sizes, while articulating a single set of connective structures useable with the varying sizes of CSPs. Thus, a single set of connective structures such as flex circuits 30 and 32 (or a single flexible circuit in the mode where a single flex is used in place of the flex circuit pair 30 and 32) may be devised and used with the form standard 34 method and/or systems disclosed herein to create stacked modules from CSPs having different sized packages. This will allow the same flexible circuitry set design to be employed to create iterations of a stacked module 10 from constituent CSPs having a first arbitrary dimension X across attribute Y (where Y may be, for example, package width), as well as modules 10 from constituent CSPs having a second arbitrary dimension X prime across that same attribute Y. Thus, CSPs of different sizes may be stacked into modules 10 with the same set of connective structures

(i.e. flex circuitry). In a preferred embodiment, form standard 34 will present a lateral extent broader than the upper major surface of the CSP over which it is disposed. Thus, the CSPs from one manufacturer may be aggregated into a stacked module 10 with the same flex circuitry used to aggregate CSPs from another manufacturer into a different stacked module 10 despite the CSPs from the two different manufacturers having different dimensions.

[0030] Further, as those of skill will recognize, mixed sizes of CSPs may be implemented into the same module 10, such as would be useful to implement embodiments of a system-on-a-stack such as those disclosed in co-pending application U.S. Pat. App. No. 10/136,890, filed May 2, 2002, which is hereby incorporated by reference and commonly owned by the assignee of the present application.

[0031] Preferably, portions of flex circuits 30 and 32 are fixed to form standard 34 by adhesive 35 which is preferably a tape adhesive, but may be a liquid adhesive or may be placed in discrete locations across the package. Preferably, adhesive 35 is thermally conductive.

[0032] In a preferred embodiment, flex circuits 30 and 32 are multi-layer flexible circuit structures that have at least two conductive layers examples of which are those described in U.S. App. No. 10/005,581, now U.S. Pat. No. 6,576,992, which has been incorporated by reference herein. Other embodiments may, however, employ flex circuitry, either as one circuit or two flex circuits to connect a pair of CSPs, that have only a single conductive layer.

[0033] Preferably, the conductive layers employed in flex circuitry of module 10 are metal such as alloy 110. The use of plural conductive layers provides advantages and the creation of a distributed capacitance across module 10 intended to reduce noise or bounce effects that can, particularly at higher frequencies, degrade signal integrity, as those of skill in the art will recognize.

[0034] Module 10 of Fig. 1 has plural module contacts 38 collectively identified as module array 40. Connections between flex circuits are shown as being implemented with low profile inter-flex contacts 42 which are, in preferred embodiments, low profile contacts comprised of solder-combined with pads and/or rings such as the flex contacts 44 shown in Fig. 3 or flex contacts 44 with orifices as shown in Fig. 4 being just examples.

[0035] Form standard 34, as employed in one preferred embodiment, is approximately 5 mils in thickness, while flex circuits 30 and 32 are typically thinner than 5 mils. Thus, the depiction of Fig. 1 is not to scale.

[0036] Fig. 2 illustrates an exemplar two-high module 10 devised in accordance with a preferred embodiment of the present invention. The depiction of Fig. 2 identifies two areas "A" and "B", respectively, that are shown in greater detail in later figures. In later Figs. 3 and 4, there are shown details of two alternative embodiments for the area marked "A" in Fig. 2. It should be understood that many different connection alternatives are available and within the scope of the invention. Fig. 5 depicts details of the area marked "B" in Fig. 2.

[0037] Fig. 3 depicts, in enlarged view, one alternative for structures that may be used in the area marked "A" in Fig. 2. Fig. 3 depicts an example preferred connection between an example low profile contact 28 and module contact 38 through flex contact 44 of flex 32 to illustrate a solid metal path from level one CSP 18 to module contact 38 and, therefore, to an application PWB or memory expansion board to which module 10 is connectable.

[0038] Flex 32 is shown in Fig. 3 to be comprised of multiple conductive layers. This is merely an exemplar flexible circuitry that may be employed with the present invention. A single conductive layer and other variations on the flexible circuitry may, as those of skill will recognize, be employed to advantage in alternative embodiments of the present invention.

[0039] Flex 32 has a first outer surface 50 and a second outer surface 52. Preferred flex circuit 32 has at least two conductive layers interior to first and second outer surfaces 50 and 52. There may be more than two conductive layers in flex 30 and flex 32 and other types of flex circuitry may employ only one conductive layer. In the depicted preferred embodiment, first conductive layer 54 and second conductive layer 58 are interior to first and second outer surfaces 50 and 52. Intermediate layer 56 lies between first conductive layer 54 and second conductive layer 58. There may be more than one intermediate layer, but one intermediate layer of polyimide is preferred. The designation "F" as shown in Fig. 3 notes the thickness "F" of flex circuit 32 which, in preferred embodiment, is approximately 3 mils. Thinner flex circuits may be employed, particularly where only one conductive layer is employed, and flex circuits thicker than 3 mils may also be employed, with commensurate addition to the overall height of module 10.

[0040] As depicted in Fig. 3 and seen in more detail in Figs. found in U.S. App. No. 10/005,581, now U.S. Pat. No. 6,576,992, which has been incorporated by reference, an example flex contact 44 is comprised from metal at the level of second conductive layer 58 interior to second outer surface 52.

[0041] Fig. 4 depicts an alternative structure for the connection in the area marked "A" in Fig. 2. In the depiction of Fig. 4, a flex contact 44 is penetrated by orifice 59 which has a median opening of dimension "DO" indicated by the arrow in Fig. 4. Demarcation gap 63 is shown in Fig. 4. This gap which is further described in incorporated U.S. Pat. App. No. 10/005,581, now U.S. Pat. No. 6,576,992, may be employed to separate or demarcate flex contacts such as flex contact 44 from its respective conductive layer. Also shown in Fig. 4 is an optional adhesive or conformed material 51 between flex circuit 32 and CSP 18.

[0042] The consolidated contact 61 shown in Fig. 4 provides connection to CSP 18 and passes through orifice 59. Consolidated contact 61 may be understood to

have two portions 61A that may be identified as an "inner" flex portion and, 61B that may be identified as an "outer" flex portion, the inner and outer flex portions of consolidated contact 61 being delineated by the orifice. The outer flex portion 61B of consolidated contact 61 has a median lateral extent identified in Fig. 4 as "DCC" which is greater than the median opening "DO" of orifice 59. The depicted consolidated contact 61 is preferably created in a preferred embodiment, by providing a CSP with ball contacts. Those ball contacts are placed adjacent to flex contacts 44 that have orifices 59. Heat sufficient to melt the ball contacts is applied. This causes the ball contacts to melt and reflow in part through the respective orifices 59 to create emergent from the orifices, outer flex portion 61B, leaving inner flex portion 61A nearer to lower surface 22 of CSP 18.

[0043] Thus, in the depicted embodiment, module 10 is constructed with a level one CSP 18 that exhibits balls as contacts, but those ball contacts are re-melted during the construction of module 10 to allow the solder constituting the ball to pass through orifice 59 of the respective flex contact 44 to create a consolidated contact 61 that serves to connect CSP 18 and flex circuitry 32, yet preserve a low profile aspect to module 10 while providing a contact for module 10. Those of skill will recognize that this alternative connection strategy may be employed with any one or more of the CSPs of module 10.

[0044] As those skilled will note, a consolidated contact 61 may be employed to take the place of a low profile contact 28 and module contact 38 in the alternative embodiments. Further, either alternatively, or in addition, a consolidated contact 61 may also be employed in the place of a low profile contact 28 and/or an inter-flex contact 42 in alternative embodiments where the conductive layer design of the flex circuitry will allow the penetration of the flex circuitry implicated by the strategy.

[0045] Fig. 5 depicts the area marked "B" in Fig. 2. The depiction of Fig. 5 includes approximations of certain dimensions of several elements in a preferred embodiment of module 10. It must be understood that these are just examples relevant to some preferred embodiments, and those of skill will immediately recognize that the invention may be implemented with variations on these dimensions and with and without all the elements shown in Fig. 5.

[0046] There are a variety of methods of creating low profile contacts 28. One method that is effective is the screen application of solder paste to the exposed CSP contact pad areas of the CSP and/or to the contact sites of the flex circuitry. For screened solder paste, the reflowed joint height of contact 28 will typically be between 0.002" and 0.006" (2 to 6 mils). The stencil design, the amount of solder remaining on 'ball-removed' CSPs, and flex planarity will be factors that could have a significant effect on this value. Low profile contact 28 has a height "C" which, in a preferred embodiment, is between 2 and 7 mils. Flex circuitry 32, with one or two or more conductive layers, has a thickness "F" of about 4 mils or less in a preferred embodiment. Adhesive layer 35 has a thickness "A1" of between 1 and 1.5 mils in a preferred embodiment. Form standard 34 has a thickness "FS" of between 4 and 6 mils in a preferred embodiment and, adhesive layer 36 has a thickness "A2" of between 1 and 2 mils. Thus, the total distance between lower surface 22 of CSP 16 and upper surface 20 of CSP 18 passing through one of low profile contacts 28 of CSP 16 is *approximated* by the formula:

(1) (C+F+A1+FS+ A2) – distance low profile contact 28 penetrates into flex 32.

In practice, this should be approximately between 9 and 20 mils in a preferred embodiment. A similar calculation can be applied to identify the preferred distances between, for example, CSP 14 and CSP 16 in a four-high module 10. In

such cases, the height of inter-flex contact 42 and thickness of another layer of flex circuit 32 will be added to the sum to result in a preferred range of between 13 and 31 mils. It should be noted that in some embodiments, not all of these elements will be present, and in others, added elements will be found. For example, some of the adhesives may be deleted, and form standard 34 may be replaced or added to with a heat spreader 37 and, in still other versions, neither a form standard 34 nor a heat spreader 37 will be found. As an example, where there is no use of a heat spreader 37 or form standard 34, the distance between lower surface 22 of CSP 16 and upper surface 20 of CSP 18 in a two-element module 10 will be preferably between 4.5 and 12.5 mils and more preferably less than 11 mils.

[0047] It is often desirable, but not required, to create low profile contacts 28 and low profile inter-flex contacts 42 using HT joints as described in co-pending application U.S. Pat. App. No. 10/457,608 which is incorporated by reference herein and is commonly-owned by the assignee of the present invention.

[0048] Fig. 6 depicts a plan view of a contact structure in flex 32 that may be employed to implement the consolidated contact 61 shown earlier in Fig. 4. Shown in Fig. 6 are two exemplar flex contacts 44 that each have an orifice 59. It may be considered that flex contacts 44 extend further than the part visible in this view as represented by the dotted lines that extend into traces 45. The part of flex contact 44 visible in this view is to be understood as being seen through windows in other layers of flex 32 as described in the incorporated by reference application U.S. Pat. App. No. 10/005,581, now U.S. Pat. No. 6,576,992, depending upon whether the flex contact is articulated at a first conductive layer or, if it is present in flex 32, a second conductive layer and intermediate layer and whether the flex contact is for connection to the lower one of two CSPs or the upper one of two CSPs in a module 10.

[0049] Fig. 7 depicts a flexible circuit connective set of flex circuits 30 and 32 that has a single conductive layer 64. It should be understood with reference to Fig. 6, that flex circuits 30 and 32 extend laterally further than shown and have portions which are, in the construction of module 10, brought about and disposed above the present, heat spreader 37, a form standard 34 (not shown), and/or upper surface 20 of CSP 18. In this single conductive layer flex embodiment of module 10, there are shown first and second outer layers 50 and 52 and intermediate layer 56.

[0050] Heat spreader 37 is shown attached to the body 27 of first level CSP 18 through adhesive 36. In some embodiments, a heat spreader 37 or a form standard 34 may also be positioned to directly contact body 27 of the respective CSP.

[0051] Heat transference from module can be improved with use of a form standard 34 or a heat spreader 37 comprised of heat transference material such as a metal and preferably, copper or a copper compound or alloy, to provide a significant sink for thermal energy. Although the flex circuitry operates as a heat transference material, such thermal enhancement of module 10 particularly presents opportunities for improvement of thermal performance where larger numbers of CSPs are aggregated in a single stacked module 10.

[0052] Although the present invention has been described in detail, it will be apparent to those skilled in the art that the invention may be embodied in a variety of specific forms and that various changes, substitutions and alterations can be made without departing from the spirit and scope of the invention. The described embodiments are only illustrative and not restrictive and the scope of the invention is, therefore, indicated by the following claims.